REPLACEMENT ABSTRACT

~~The invention provides a~~ A parallel data processing device having an array of parallel processing elements ~~(LPA1...320)~~ for processing a signal to obtain parallel streams of data~~, and means (TSMM1...80) for shuffling~~ includes a dada shuffler configured to shuffle the parallel streams of data in a block-wise manner. The data ~~shuffling means (TSMM1...80) have~~ shuffler has an array of addressable switch memory matrices ~~(TSMM1...80)~~ which are each coupled to a predetermined number of processing elements ~~(LPA1...320)~~. The array of switch memory matrices ~~(TSMM1...80)~~ solves data flow limitations of highly parallel linear array processors as well as intermediate storage requirements of image processing algorithms. In a camera system, the parallel data processing device is combined with a sensor array ~~(S)~~.

~~Fig. 1~~